REMARKS

This paper is responsive to a Non-Final Office action dated December 14, 2007. Claims 1-5, 7-34, 36-39, 41-46, and 48-60 were examined.

Objections to the Drawings

The drawings are objected to under 37 C.F.R. 1.83(a). Applicants respectfully maintain that the drawings satisfy the requirements of 37 C.F.R. 1.83(a).

Regarding claim 1, Applicants respectfully point to at least the electromagnetic shielding structure formed by top plate 552, bottom plate 508, sidewalls 556 and 550, and rows of vias 564 and 562 of Fig. 5B, which illustrates at least one embodiment of

> the electromagnetic shielding structure formed at least partially in one or more redistribution layers formed on an integrated circuit die, the electromagnetic shielding structure substantially surrounding a circuit element,

required by claim 1.

Applicants respectfully point to at least top plate 552, sidewalls 556 and 550, and the region between sidewalls 556 and 550 of Fig. 5B, which illustrate at least one embodiment of

> the redistribution layers including at least one redistribution metal layer and at least one redistribution dielectric layer,

as required by claim 1.

Applicants respectfully point to at least the region between sidewalls 556 and 550 and the region between rows of vias 564 and 562 of Fig. 5B, which illustrate at least one embodiment of

> a redistribution dielectric layer that is at least 5um thick and a dielectric layer of the integrated circuit die that is less than 1um thick,

as required by claim 1.

Regarding claim 3, Applicants respectfully point to at least top plate 552, sidewalls 556, and sidewalls 550 of Fig. 5B, which illustrate at least one embodiment of

> redistribution layers formed above a passivation layer of the integrated circuit die,

as required by claim 3.

Regarding claim 4, Applicants respectfully point to at least top plate 552 of the electromagnetic shielding structure formed by top plate 552, bottom plate 508, sidewalls 556 and 550, and rows of vias 564 and 562 of Fig. 5B, which illustrates at least one embodiment of

> redistribution layers formed above integrated circuit pads,

as required by claim 4.

Accordingly, Applicants believe that the drawings satisfy the requirements of 37 C.F.R. 1.83(a). Applicants respectfully request that the objections to the drawings be withdrawn.

Claim Rejections Under 35 U.S.C. § 112

Claims 1-5, 7-34, 36-39, 41-46, and 48-60 stand rejected to under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. In particular, the Office action states that it is unclear how the shielding structure is formed at least partially in one or more redistribution layers. Applicants respectfully point out that definiteness of claim language is determined based on "whether those skilled in the art would understand what is claimed when the claim is read in light of the specification." See Bancorp Services LLC v. Hartford Life Ins. Co., 69 USPQ2d 1996, 1999 (Fed. Cir. 2004) (emphasis added); see also MPEP § 2173.02. Note

that "a claim is not indefinite merely because it poses a difficult issue of claim construction; if the claim is subject to construction, i.e., it is not insolubly ambiguous, it is not invalid for indefiniteness." See Bancorp, 69 USPQ2d at 1999. Applicants respectfully maintain that claims 1-5, 7-34, 36-39, 41-46, and 48-60, satisfy this requirement. Furthermore, Applicants note that a shielding structure formed at least partially in one or more redistribution layers is fully described in the specification. Applicants respectfully point the Examiner to at least Figures 5A and 5B and associated portions of the specification, which state:

> Referring to FIG. 5A, an exemplary integrated circuit die cross-section 500 illustrates a Faraday cage surrounding an inductor structure. The Faraday cage includes top plate 502 formed in a redistribution layer by, e.g., under bump metallurgy. Bottom plate 508 and sidewall portions 554 and 552 are formed in typical integrated circuit layers. Support structures 556 and 550 are formed in redistribution layers. Although bottom plate 508 is illustrated as formed in a first metal layer of the typical integrated circuit process, bottom plate 508 may be formed with a combination of a first and second metal layer of the typical integrated circuit process, in a redistribution layer, or in any other suitable layer or combination of layers. In the illustrated embodiment, inductor structure 525 is formed in the first two conductive redistribution layers 526 and 528. Inductor structure 525 is electrically coupled to other circuitry on the integrated circuit die by contacts 530 and 532. However, the inductor structure may be formed in any suitable redistribution layers, typical integrated circuit layers, or any combination thereof.
>
> In an exemplary embodiment, rows of vias in the typical integrated circuit layers, e.g., rows 554 and 552, are electrically coupled to sidewalls formed in a structure formed of under bump metallurgy (e.g., sidewalls 504 and 548). These sidewalls are formed by a non-planar layer of under bump metallurgy (e.g., the non-planar layer including top-plate 502 and sidewalls 504 and 548) that is supported by via structures e.g., support structures 556 and 550, formed in the redistribution layers. The sidewalls are

> coupled to portions of the Faraday cage formed in the typical integrated circuit layers, e.g., by coupling metal layer 534 in the redistribution process to metal layer 538 in the typical integrated circuit process with conductive via 536.
>
> Referring to FIG 5B, another exemplary integrated circuit die cross-section 550 illustrates a Faraday cage surrounding an inductor structure (i.e., inductor 525). Top plate 552 is formed in a redistribution layer by, e.g., under bump metallurgy. Sidewalls 556 and 550 are formed in redistribution layers. Rows of vias in the typical integrated circuit layers, e.g., rows 564 and 562, are electrically coupled to sidewalls 556 and 550.

Paragraphs 1050-1052 (emphasis added). Applicants respectfully maintain that the limitations requiring that an electromagnetic shielding structure formed at least partially in one or more redistribution layers formed on an integrated circuit, satisfies the requirements of 35 U.S.C. § 112, second paragraph. Accordingly, Applicants respectfully request that the rejection under 35 U.S.C. § 112, second paragraph, of claims 1, 11, 13, 29, 41, and 48 and all claims dependent thereon, be withdrawn.

Claim 13 is amended to correct a typographical error. Applicants believe that amended claim 13 satisfies the requirements of 35 U.S.C. § 112, second paragraph. Accordingly, Applicants respectfully request that the rejection under 35 U.S.C. § 112, second paragraph, of claim 13 be withdrawn.

Claim Rejections Under 35 U.S.C. § 102

Claims 13 and 14 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,037,649 to Liou (hereinafter "Liou"). Regarding claim 13, Applicants respectfully maintain that Liou, alone or in combination with other references of record, fails to teach or suggest

> an electromagnetic shielding structure formed at least partially in one or more redistribution layers formed on an integrated circuit die, the electromagnetic

> shielding structure substantially surrounding a circuit element,

as required by claim 13. Liou teaches a three-dimensional inductor structure formed in a conventional integrated circuit technology. Abstract. Liou teaches further that "[t]hree levels of metal lines are separated from one another by isolating layers." Col. 2, lines 34-36. Two nearby levels of metal lines of Liou are interconnected through via plugs in the isolating layer between them. Col. 2, lines 36-37. The first isolating layer of Liou is directly formed on a substrate. Col. 3, lines 41-42. The third-level metal lines of Liou and the pads are formed on the third isolating layer. Col. 4, lines 25-26.

In contrast, claim 13 requires an electromagnetic shielding structure formed at least partially in one or more redistribution layers formed on an integrated circuit die. Applicants respectfully point out that

> [r]edistribution layers may be any layers formed on the integrated circuit used to route electrical connections between contact pads on an IC die and a location of a package contact. This may include depositing and patterning metal layers to transform an existing input/output layout into a pattern that satisfies the requirements of a solder bump design.
>
> The redistribution layers are typically formed above a passivation layer, i.e., a layer formed on an integrated circuit to provide electrical stability by protecting the integrated circuit from moisture, contamination particles, and mechanical damage. The passivation layer may include silicon dioxide, silicon nitride, polyimide, or other suitable passivation materials. Redistribution layers are typically formed above integrated circuit bonding pads. These pads, typically coupled to an electronic device formed in the integrated circuit, may include aluminum, copper, titanium, or other suitable material. However, redistribution layers may include additional dielectric and conductive layers formed on an integrated circuit die in the absence of a passivation layer or bonding pads.

> Redistribution layers typically have thicknesses substantially greater than the thicknesses of typical dielectric and conductive layers formed on an integrated circuit die. For example, a typical conductive layer in an integrated circuit is less than 1μm thick and corresponding dielectric layers are also less than 1μm thick. However, conductive layers in an exemplary redistribution layer are at least 2μm thick and corresponding dielectric layers are at least 5μm thick. In another embodiment, the dielectric layers are at least 15μm thick. Redistribution dielectric layers may include silicon nitride, oxynitride, silicon oxide, benzocyclobutene (BCB), polyimide, or other suitable materials. Redistribution conductive layers may include aluminum, copper, or other suitable materials.
>
> In an exemplary embodiment, Faraday cage 233 includes a solid top plate 230, formed in a conductive redistribution layer. Top plate 230 may be formed from a redistribution conductor layer (e.g., copper or aluminum) or under bump metallurgy. Under bump metallurgy typically provides a connection between a solder bump and a contact pad and provides a surface to which solder will adhere. The under bump metallurgy may include titanium, copper, nickel, gold, chromium and/or other suitable materials.

Paragraphs 1041-1044. The three levels of metal lines and three isolating layers of Liou are not redistribution layers, as required by claim 13. Nowhere does Liou teach or suggest redistribution layers, or an electromagnetic shielding structure formed at least partially in one or more redistribution layers formed on an integrated circuit die, as required by claim 13.

For at least these reasons, Applicants respectfully maintain that claim 13 distinguishes over Liou and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 13 and all claims dependent thereon, be withdrawn.

Claim Rejections Under 35 U.S.C. § 103

Claims 11-12 and 18 stand rejected under 35 U.S.C. § 103(a) as being anticipated by Liou in view of U.S. Patent No. 6,847,282 (hereinafter "Gomez").

Regarding claim 11, Applicants respectfully maintain that Liou, alone or in combination with Gomez or other references of record, fails to teach or suggest

> an electromagnetic shielding structure formed at least partially in one or more redistribution layers and having a top plate, a bottom plate, and sidewalls, the top plate and at least a portion of the sidewalls being formed by under bump metal,

as required by claim 11. Liou teaches a three-dimensional inductor structure formed in a conventional integrated circuit technology. Abstract. Liou teaches further that "[t]hree levels of metal lines are separated from one another by isolating layers." Col. 2, lines 34-36. Two nearby levels of metal lines of Liou are interconnected through via plugs in the isolating layer between them. Col. 2, lines 36-37. The first isolating layer of Liou is directly formed on a substrate. Col. 3, lines 41-42. The third-level metal lines of Liou and the pads are formed on the third isolating layer. Col. 4, lines 25-26.

In contrast, claim 11 requires an electromagnetic shielding structure formed at least partially in one or more redistribution layers and having a top plate, a bottom plate, and sidewalls, the top plate and at least a portion of the sidewalls being formed by under bump metal. Applicants respectfully point out that

> [r]edistribution layers may be any layers formed on the integrated circuit used to route electrical connections between contact pads on an IC die and a location of a package contact. This may include depositing and patterning metal layers to transform an existing input/output layout into a pattern that satisfies the requirements of a solder bump design.

The redistribution layers are typically formed above a passivation layer, i.e., a layer formed on an integrated circuit to provide electrical stability by protecting the integrated circuit from moisture, contamination particles, and mechanical damage. The passivation layer may include silicon dioxide, silicon nitride, polyimide, or other suitable passivation materials. Redistribution layers are typically formed above integrated circuit bonding pads. These pads, typically coupled to an electronic device formed in the integrated circuit, may include aluminum, copper, titanium, or other suitable material. However, redistribution layers may include additional dielectric and conductive layers formed on an integrated circuit die in the absence of a passivation layer or bonding pads.

Redistribution layers typically have thicknesses substantially greater than the thicknesses of typical dielectric and conductive layers formed on an integrated circuit die. For example, a typical conductive layer in an integrated circuit is less than 1μm thick and corresponding dielectric layers are also less than 1μm thick. However, conductive layers in an exemplary redistribution layer are at least 2μm thick and corresponding dielectric layers are at least 5μm thick. In another embodiment, the dielectric layers are at least 15μm thick. Redistribution dielectric layers may include silicon nitride, oxynitride, silicon oxide, benzocyclobutene (BCB), polyimide, or other suitable materials. Redistribution conductive layers may include aluminum, copper, or other suitable materials.

In an exemplary embodiment, Faraday cage 233 includes a solid top plate 230, formed in a conductive redistribution layer. Top plate 230 may be formed from a redistribution conductor layer (e.g., copper or aluminum) or under bump metallurgy. Under bump metallurgy typically provides a connection between a solder bump and a contact pad and provides a surface to which solder will adhere. The under bump metallurgy may include titanium, copper, nickel, gold, chromium and/or other suitable materials.

Paragraphs 1041-1044. The three levels of metal lines and three isolating layers of Liou are not redistribution layers or under bump metal, as required by claim 11. Nowhere does Liou teach or suggest redistribution layers or under bump metal, or an electromagnetic shielding structure formed at least partially in one or more redistribution layers and having a top plate, a bottom plate, and sidewalls, the top plate and at least a portion of the sidewalls being formed by under bump metal, as required by claim 11.

Gomez fails to compensate for the shortcomings of Liou. Gomez teaches a substrate having a plurality of layers that each have a corresponding surface. Col. 3, lines 28-38. A conductive bottom shield pattern of Gomez is disposed on a third surface and a conductive top shield pattern is disposed on a fourth surface. Col. 5, lines 11-18. Gomez fails to teach or suggest that the surfaces and layers of Gomez are redistribution layers or under bump metal, as required by claim 11. Nowhere does Gomez teach or suggest redistribution layers or under bump metal, or an electromagnetic shielding structure formed at least partially in one or more redistribution layers and having a top plate, a bottom plate, and sidewalls, the top plate and at least a portion of the sidewalls being formed by under bump metal, as required by claim 11.

For at least these reasons, Applicants respectfully maintain that claim 11 distinguishes over Liou, Gomez and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 11 and all claims dependent thereon, be withdrawn.

Additional Remarks

Claims 41 and 52 are amended to correct typographical errors.

In summary, claims 1-5, 7-34, 36-39, 41-46, and 48-60 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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Respectfully submitted,

Nicole Teitler Cave

Nicole Teitler Cave, Reg. No. 54,021
Attorney for Applicant(s)
(512) 338-6315 (direct)
(512) 338-6300 (main)
(512) 338-6301 (fax)